Risk Assessment

Summary

Reference: **RA030726/1** **Sign-off Status:** **Authorised**

Date Created:	09/10/2019	**Confidential?**	No
Assessment Title:	3rd year project: Performance characterisation of 8-bit RISC and OISC architectures		
Assessment Outline:	New activity		

Area Responsible (for management of risks)		**Location of Risks**	On-Site
Division, School, Faculty, Institute:	Faculty of Engineering Science	**Building:**	Roberts Building
Department:	Dept of Electronic & Electrical Eng	**Area:**	Ground and Above
Group/Unit:	All Groups/Units	**Sub Area:**	Laboratory

Further Location Information:	Roberts building Rooms 704, 905. Also working from home.		
Assessment Start Date:	09/10/2019	**Review or End Date:**	31/03/2020

Relevant Attachments:

Description of attachments:

Location of non-electronic documents:

Assessor(s):	Jarmolovicius, Min
Approver(s):	ROBERT KILLEY
Signed Off:	ROBERT KILLEY (09/10/2019 12:56)
Distribution List:	Gerald McBrearty (g.mcbrearty@ucl.ac.uk) - 09/10/2019 ANDREW MOSS (andrew.moss@ucl.ac.uk) - 09/10/2019

PEOPLE AT RISK (from the Activities covered by this Risk Assessment)

CATEGORY
Undergraduates

Risk Assessment

Activities, Hazards, Controls

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1. Working in a lab

Description of Activity:

Hazard 1. Using computer

RSI Eye strain Bad posture	**Existing Control Measures** Properly use mouse/keyboard Make constant breaks Make sure sit properly

Hazard 2. Testing FPGA

Burns from hot wires/chips due to short-circuits	**Existing Control Measures** Use current limit on power supplies

Risk Level

With Existing Controls:

Risk Level **A - Very Low / Trivial**