University College London

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Project Progress Report No. 3

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1 Progress

The following points have been done since last report:

- New instruction have been added to RISC;
- Implemented multiple function in assembly for RISC;
- Improved RISC assembler;
- Started to implement the structure of OISC in SystemVerilog;

Project schedule as Grantt chart has been updated in the last page in table 2.

1.1 New RISC instruction

Added `ADDC` and `SUBC` instructions to allow addition and subtraction with carry. They work as follows:
`ADDC [operand]`: operand = operand + carry
`SUBC [operand]`: operand = operand - carry
Carry flag is write to only at `ADD`, `ADDI`, `SUB` and `SUBI` instructions.

Note that some instruction become unnecessary since last instruction changes, mainly `INC` and `DEC` that increase/decrease operand value by 1 This instruction can be replaced by
`ADDI [operand] 1` and `SUBI [operand] 1`
Such replacement would only have 1 downside as taking 1 byte more in instruction memory.

1.2 RISC assembly functions

Created following RISC functions in assembly:

Name	Description	Line
read_char	Waits for input from UART and writes to `r0`	922
print_char	Sends `r0` byte to print to UART	964
print_msg	Prints string to UART from memory pointer at `{r2 r1}`	944
printU8	Prints unsigned 8bit decimal at `r0` to UART	783
printU16	Prints unsigned 16bit decimal at `{r0 r1}` to UART	741
printhex	Prints hexadecimal value at `r0` to UART	271
printbin	Prints binary value at `r0` to UART	245
mulU16	Multiples value in `{r0 r1}` with `{r2 r3}` resulting in 32bit value in `{r0 r1 r2 r3}`	655
arrayPop	Removes last value from array at memory pointer in `{r0 r1}` and places value in `{r2 r3}`	894
arrayPush	Adds value in `{r2 r3}` to array at memory pointer in `{r0 r1}`	854
arrayClear	Resets array header in memory pointer `{r0 r1}`	840
sieveOfAtkin	Calculates and prints first 255 prime numbers	375

Table 1: List of implemented RISC functions. Note Line numbers are hyperlinks to assembly file at specific commit.

1.3 RISC assembler

Assembler has `@` operator that takes nth byte from a value or label. E.g. `0x0102@n` would return nth byte of 0x0102. This is useful for decimal values.

1.4 OISC Implementation

A basic architecture of OISC processor has been implemented. The fundamental structure includes a common bus (SystemVerilog interface named *IBus*) that includes data and instruction wires. Instruction currently is 16bit wide, where first byte is destination address and second byte is source address.

Modules can be attached to IBus using Ports. Ports is SystemVerilog module that takes address as a parameter and has 2 internal registers - `data_from_bus` and `data_to_bus`. If instruction destination matches Port address data `data_from_bus` is set to IBus data value, otherwise it does not change. If instruction source matches Port address register `data_to_bus` is connected to IBus data bus, otherwise IBus data connection is set to high impedance.

Immediate value can be writing to special Port by writing instruction source address (which would be the immediate value) to `data_from_bus` instead of data bus. In such case source address might be invalid however this does not affect operation as invalid address resulting data bus being unknown state is ignored by destination.

Port and IBus are described in here.

2 Difficulties encountered

Some minor difficulties been encountered with assembler. Its been discovered that assembler had a software bug where in 2-operand instructions operand positions were swapped resulting in issues with compiler code. So far this is the only issue caused by assembler.

It also been discovered that writing assembly takes a lot of time, therefore writing a higher level compiler (e.g. BASIC) or translation program to convert RISC assembly to OISC is considered.

3 Failure Risk Assessment

There are no updates on failure risk assessment.

4 Updated Safety Risk Assessment

There are no updates on safety risk assessment.

5 Help and Advice Needed

At this state no help is needed, and any issues and advices are sorted out and discussed in weekly supervisor meetings.

6 Updated Schedule

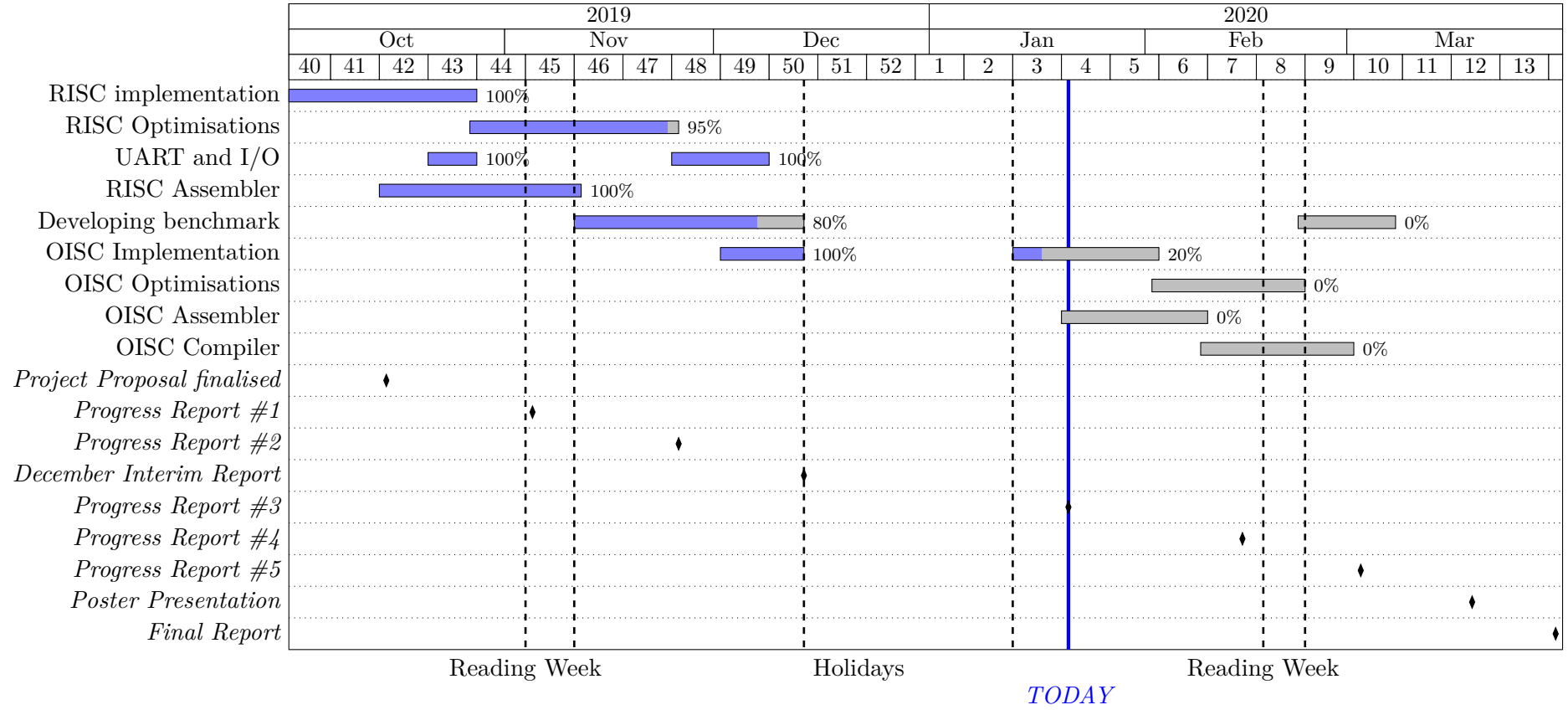

Table 2: Updated project schedule Grantt chart