University College London

Department of Electronic and Electrical Engineering

Project Progress Report No. 5

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1 Progress

Over past 2 weeks following were completed:

1.1 Prime numbers

Almost completed OISC program to calculate and efficiently store prime numbers up to 16bit, also print all of them to the terminal. Only missing loop to remove square numbers.

1.2 Debugging interface

Written debugging interface that can access verilog implemented probes and sources, as well as read and modify memory (RAM and instruction ROM) on working processor via JTAG. This enables to see internal processor state, control clock and after each step view changes in memory.

1.3 Benchmarking plan

Following benchmarks been designed to be completed until the end of project:

- Compare used LUL and registers between different blocks processor parts for both processors.
- Measure power consumption in order to estimate average energy per instruction.
- Do program simulation to find characteristic of instructions been executed on different tasks e.g. see most commonly executed instructions on 16bit division, multiplication, modulus, prime number calculator.
- Measure time that takes each task mentioned above to execute.
- If there will be enough time - test both processors critical path and estimate/test maximum frequency.

2 Difficulties encountered

Minor difficulties with time management.

3 Failure Risk Assessment

There are no updates on failure risk assessment.

4 Updated Safety Risk Assessment

There are no updates on safety risk assessment.

5 Help and Advice Needed

At this state no help is needed, and any issues and advices are sorted out and discussed in weekly supervisor meetings.

6 Updated Schedule

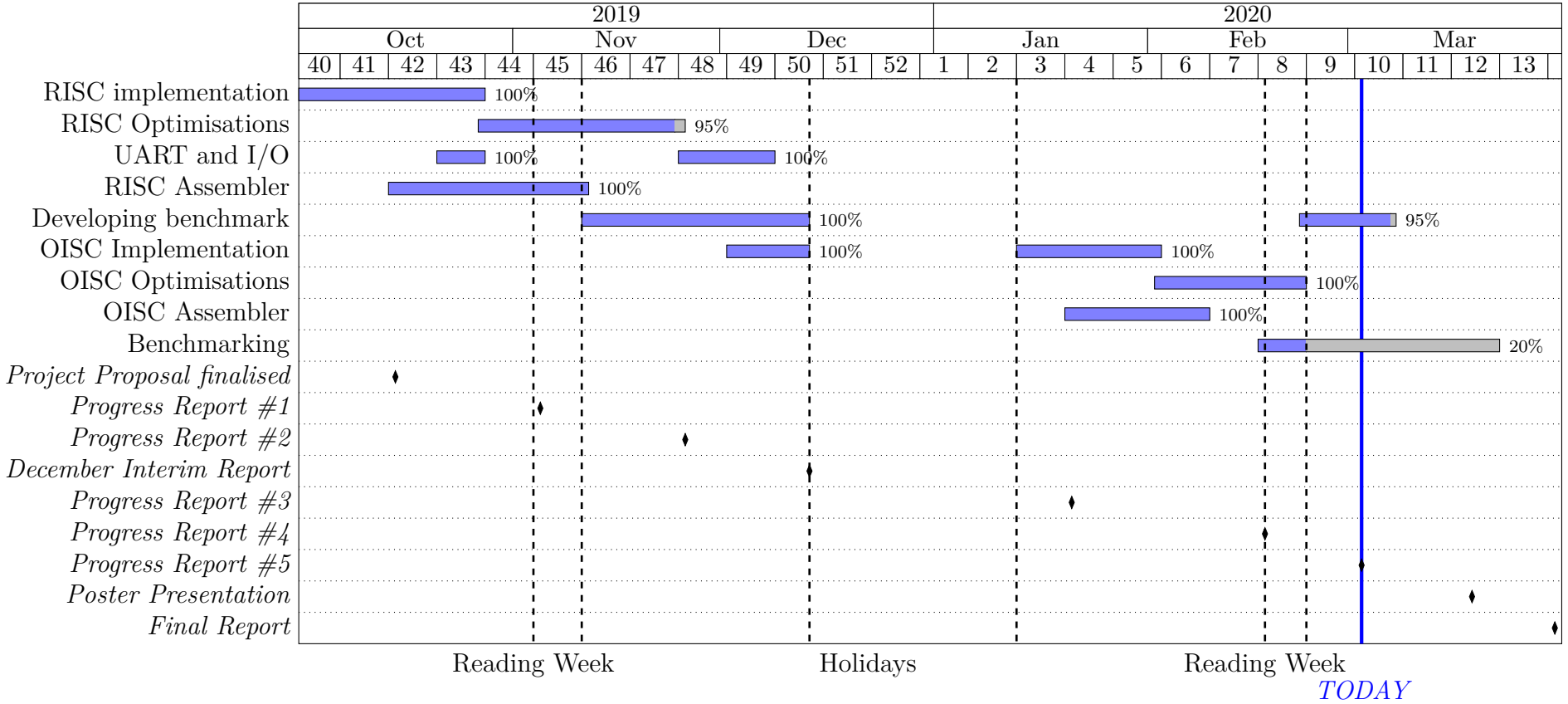

Table 1: Updated project schedule Grantt chart