Performance characterisation of 8-bit RISC and OISC architectures

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Introduction

This is a bunch of text for introductions that describes project, what it is about and that it compares RISC versus OISC architectures. Also motivation and academic papers.

RISC Architecture

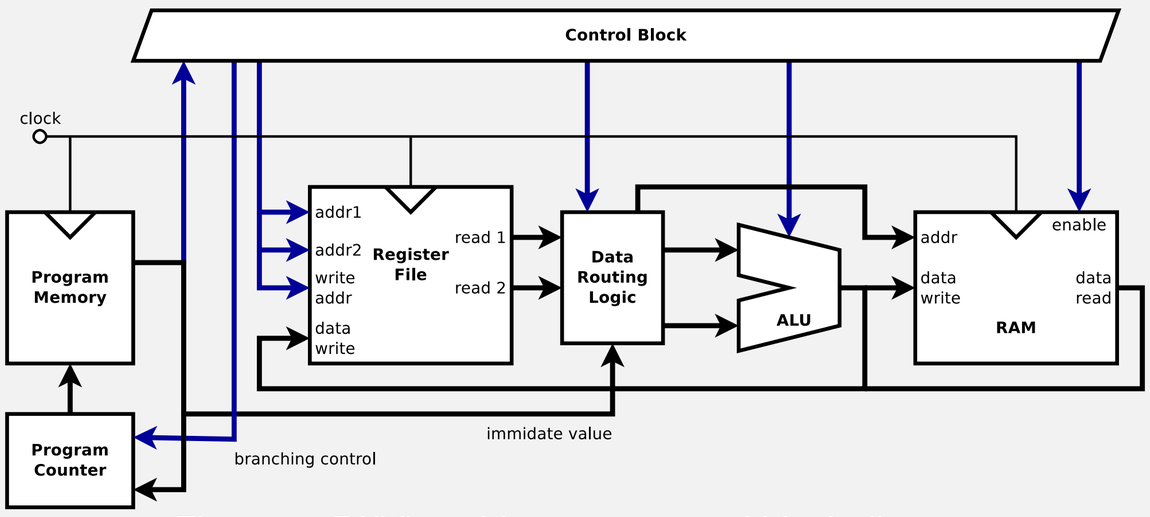

Figure 1: RISC architecture general block diagram

OISC Architecture

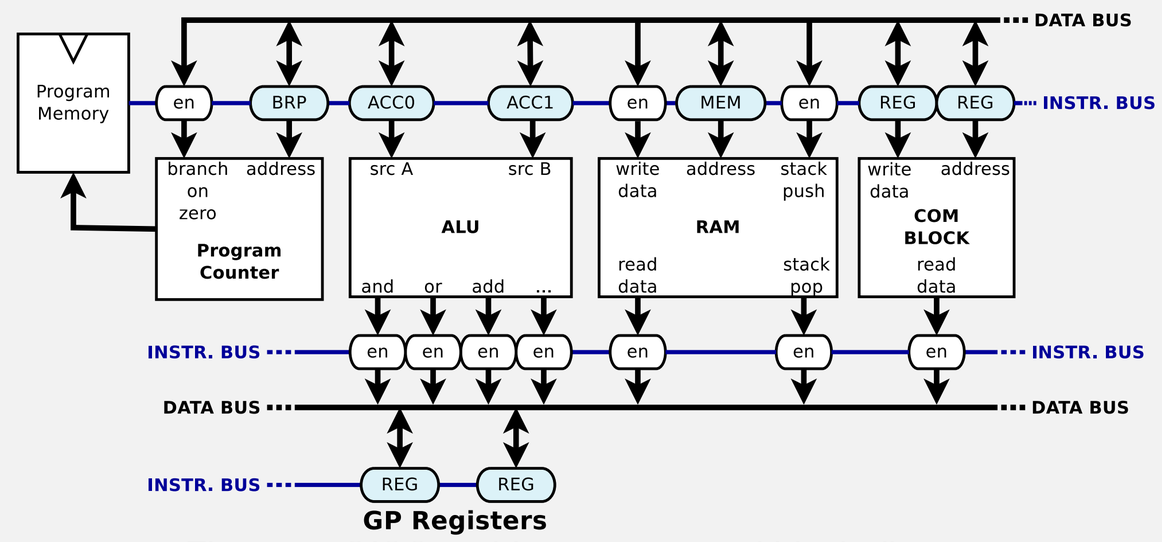

Figure 2: OISC architecture general block diagram

bit index: 0 1 2 3 4 5 6 7
op. code | dst. | src.

- 45 Instructions
-

- Bunch of instructions
- Efficient instruction space
- Generally easy to use but damn to low number of registers.
- Needs optimisation.

Machine code
OISC instruction are fixed 13bit width, 1 bit to set source as immediate value, 4bits for destination address and 8bit for source or immediate.

bit index: 0 1 2 3 4 5 6 7 8 9 10 11 12
imm. | destination | source

Total number of:

- 15 Destination addresses
- 41 Source addresses

- Only one instruction
- Not so efficient instruction space
- Takes forever to write in assembly
- Takes no time to improve. It just asking for more data buses!

Results

Following functions have been implemented in assembly:

- Print ASCII, Binary, Hexadecimal and Decimal (8 and 16bit)
- 16bit multiplication
- 16bit division
- 16bit modulus
- Sieve of Atkins (prime number calculator)

Future work

Explain future work, experiments, oisc improvements.