University College London

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Project Progress Report No. 2

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1 Progress

The following points have been done since last report:

- Upgraded assembler to support more complex operations, also changed syntax to comply with NASM;
- Upgraded automatisation using MakeFile;
- Implemented instruction memory using FPGA's M9K Memory;
- Have functional communication block, see Table 1;
- Implemented most of the instructions, see Table 2;

Address	Function	Send	Return
0x04	Read UART0 flags	-	UART0 flags
0x05	Transmit to UART0	TX byte	UART0 flags
0x06	Set DE0-Nano board LEDs	LED byte	-
0x07	Read DE0-Nano DIP switches	-	Lower DIP nibble

Table 1: Addresses and functions for communication block

Project schedule as Grantt chart has been updated in the next page in table 3.

2 Difficulties encountered

Instruction memory (ROM) has been replaced with M9K memory instead of LC (logic cell), however, as this memory is clocked it caused further problems with program counter timings.

NASM-like assembler can have multiple very useful functions such as pre-compiler, macros, imports, db instruction (stores strings) etc. It is difficult to implement all these advanced functions.

Due to scale of project, byte order has been mixed (internally processor operates at little-endian, however addresses in instructions are written as big-endian), this needs to be sorted out.

3 Failure Risk Assessment

There are no updates on failure risk assessment. As before, the most dominant failure risk is running out of time project is behind schedule.

See table 3 for schedule. In 2 weeks is scheduled to start consider OISC architecture, however, the RISC processor is still far from completion. Benchmark development might need to extended to be completed during winter holidays. Higher level RISC compiler might be replaced by advanced functions in NASM-like compiler.

4 Updated Safety Risk Assessment

There are no updates on safety risk assessment.

5 Help and Advice Needed

At this state no help is needed, and any issues and advices are sorted out and discussed in weekly supervisor meetings.

Instr.	Description	Completed
	2 register instructions	
MOVE	Copy intimidate or register	x
ADD	Arithmetical addition	x
SUB	Arithmetical subtraction	x
AND	Logical AND	x
OR	Logical OR	x
XOR	Logical XOR	x
MUL	Arithmetical multiplication	x
DIV	Arithmetical division (inc. modulus)	x
BR	Branch on registers equal	
	1 register instructions	
SLL	Shift left logical	
SRL	Shift right logical	
SRA	Shift right arithmetical	
SRAS	Shift right arithmetical signed	
LWHI	Load word (high byte)	x
SWHI	Store word (high byte, reg. only)	x
LWLO	Load word (low byte)	x
SWLO	Store word (low byte, stores high byte reg.)	x
INC	Increase by 1	x
DEC	Decrease by 1	x
GETAH	Get ALU high byte reg. (only for MUL & DIV)	x
GETIF	Get interrupt flags	
PUSH	Push to stack	x
POP	Pop from stack	x
COM	Send/Receive to/from com. block	x
SETI	Set immediate from register	
BEQ	Branch on equal	x
BGT	Branch on greater than	x
BGE	Branch on greater equal than	x
BZ	Branch on zero	x
	0 register instructions	
CALL	Call function, put return to stack	x
RET	Return from function	x
JUMP	Jump to address	x
RETI	Return from interrupt	
CLC	Clear ALU carry-in	
SETC	Set ALU carry-in	
CLS	Clear ALU sign	
SETS	Set ALU sign	
SSETS	Enable ALU sign	
CLN	Clear ALU negative	
SETN	Set ALU negative	
SSETN	Enable ALU negative	
RJUMP	Relative jump	
RBWI	Replace ALU src. B with immediate	

Table 2: Instruction set for RISC processor

6 Updated Schedule

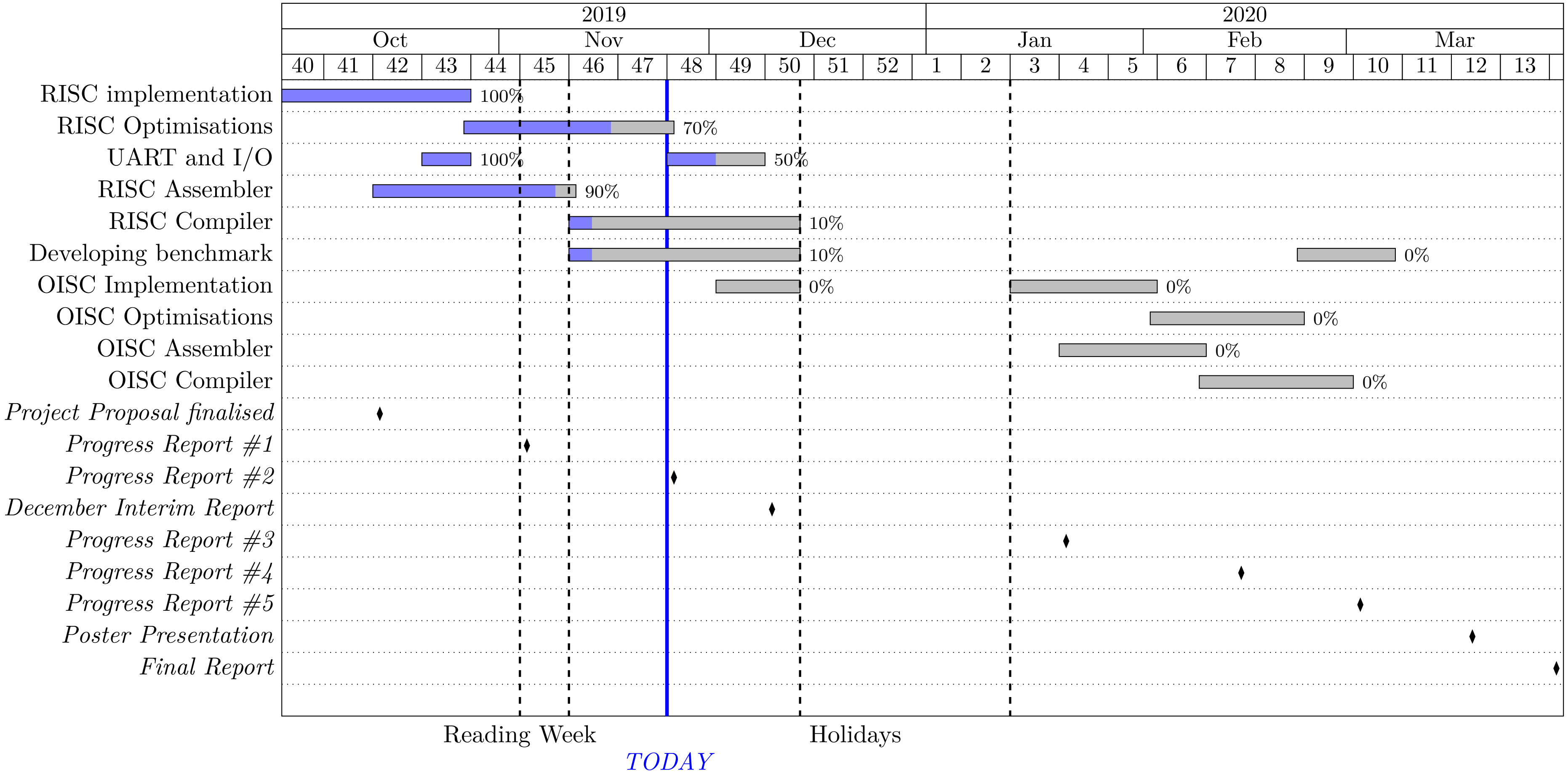

Table 3: Updated project schedule Grantt chart