University College London

Department of Electronic & Electrical Engineering

Project Progress Report No. 1

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1 Progress

The following points have been done so far:

- Finalised RISC instruction set;
- Have fundamental instructions implemented to RISC;
- Have working assembly compiler (not all instructions yet implemented);
- Implemented HDL interface allowing connecting different processors without needing to change or rewrite top level code;
- Implemented UART;
- Implemented SDRAM controller;

Project schedule as Grantt chart has been updated in the next page in table 1.

2 Difficulties encountered

Main difficulties are inexperience with SystemVerilog and structuring large hierarchical HDL code. One of more specific examples having different effects between Verilog's "wire" and "reg" or "logic" definitions causing issues between combination and sequential logics. These difficulties have been slowly resolved by learning and practising on writing code.

3 Failure Risk Assessment

There are no updated on failure risk assessment. One of the most dominant failure risk is running out of time project is a bit behind schedule.

See table 1 for schedule. Next week is scheduled RISC compiler and benchmark development, however, the RISC processor is not fully implemented which would allow writing more complicated programs, including benchmark. Therefore it is expected RISC compiler and benchmark development to be delayed by anywhere from few days up to a week.

4 Updated Safety Risk Assessment

There are no updates on safety risk assessment.

5 Help and Advice Needed

At this state no help is needed, and any small issues and advices are sorted out in weekly supervisor meetings.

6 Updated Schedule

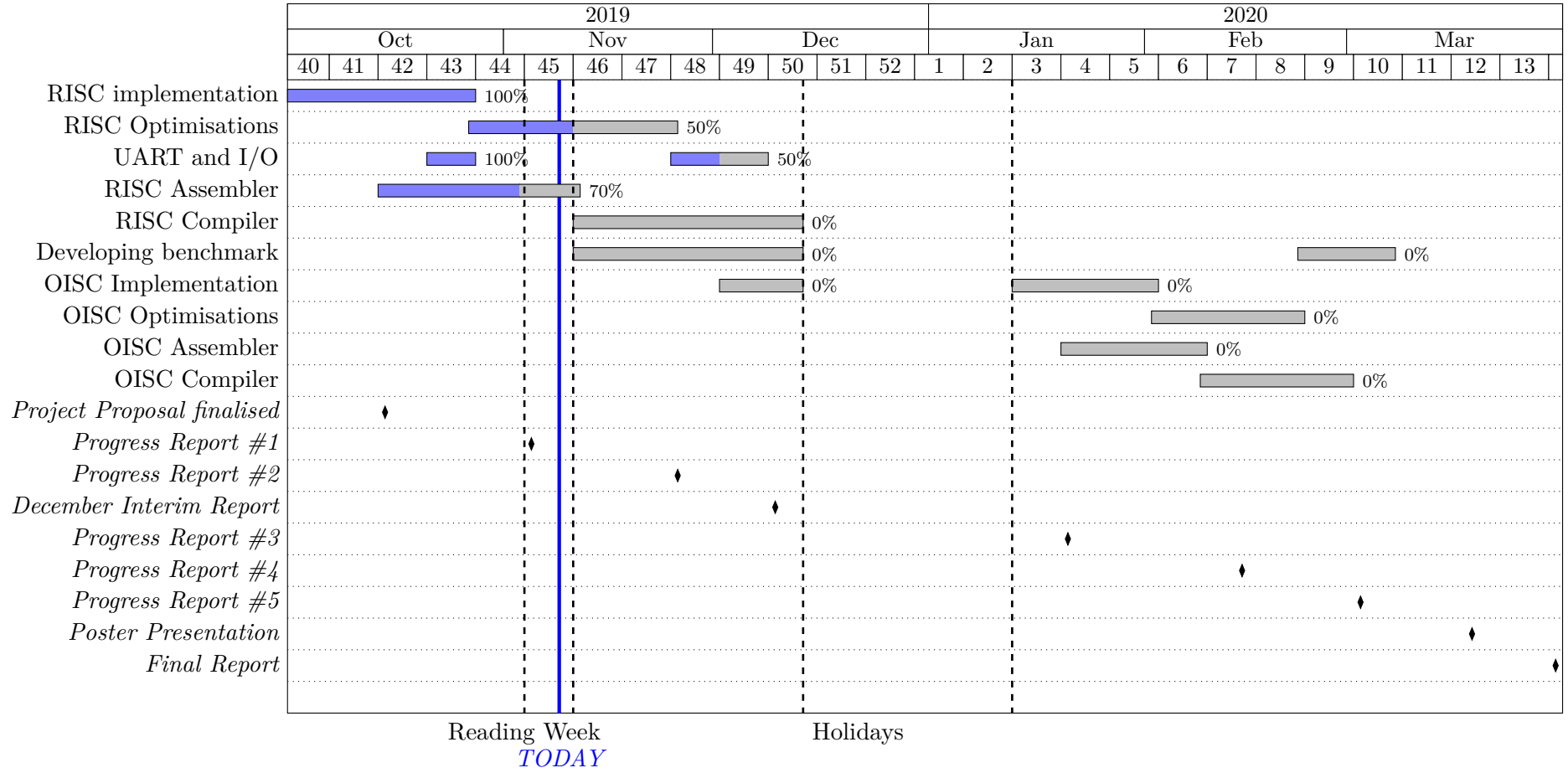

Table 1: Updated project schedule Grantt chart