Performance characterisation of 8-bit RISC and OISC architectures

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Introduction

This is a bunch of text for introductions that describes project, what it is about and that it compares RISC versus OISC architectures.

RISC

- bunch of instructions
- efficient instruction space
- generally easy to use but damn to low number of registers.
- needs optimisation.

OISC

- only one instruction
- not so efficient instruction space
- takes forever to write in assembly
- takes no time to improve. It just asking for more data buses!

Results

This is section with some results if I will have enough time to complete them.. **RIP MY FREE TIME**.

Future work

Explain future work, experiments, oisc improvements.