



UNIVERSITY COLLEGE LONDON

DEPARTMENT OF ELECTRONIC AND ELECTRICAL ENGINEERING

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## Project Progress Report No. 6

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*Author:*

Minduagas JARMOLOVILIUS  
zceemja@ucl.ac.uk

*Supervisor:*

Prof. Robert KILLEY  
r.killey@ucl.ac.uk

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# 1 Progress

Tasks that been done since last progress report:

## 1.1 Presentation and Final report

Completed presentation & started working on final project report.

## 1.2 Power measurement

Experiment been performed to measure power consumption of both processors at fixed frequency of 1MHz.

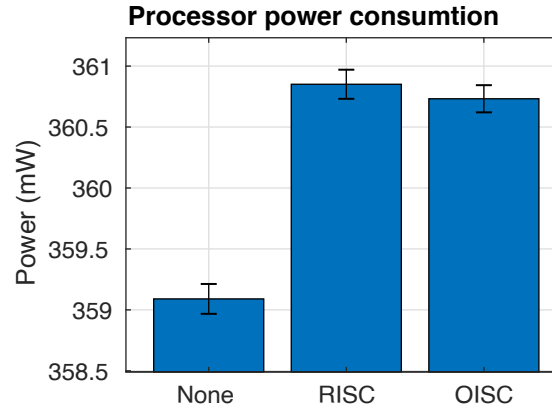


Figure 1.2.1: Measured power of processors when implemented on FPGA, running 16bit multiplication function in loop. None indicates auxiliary-only power.

## 1.3 RISC programs

Added RISC programs to calculate 16bit modulus and division. Almost completed RISC Sieve of Atkins for 16bit.

## 1.4 Function analysis

Using modelsim, performed simulations on both processors for multiple tasks. Executed instruction have been recorded and further analysed to see function instruction composition.

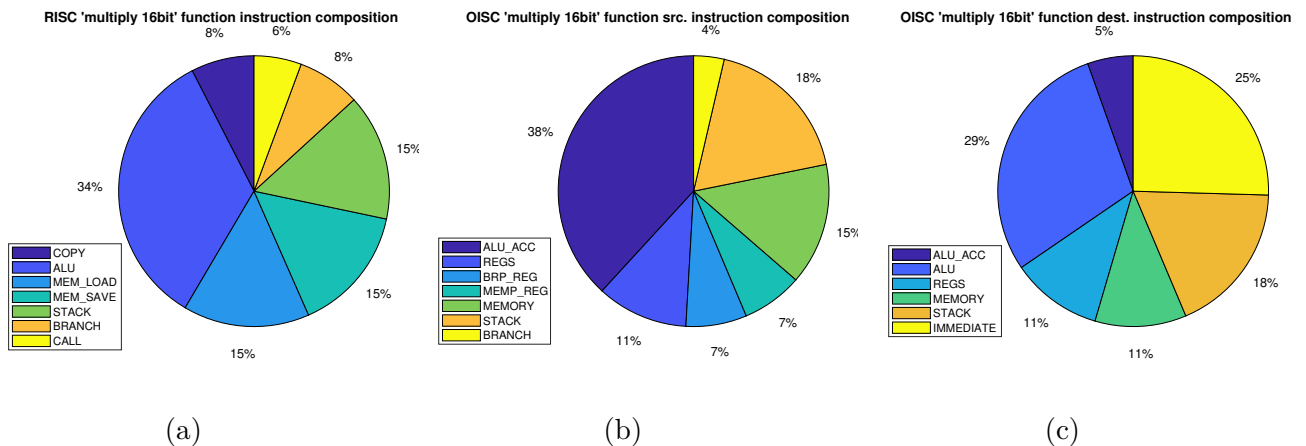


Figure 1.4.1: Instruction composition experiment results for 16bit multiplication

## 2 Difficulties encountered

When writing Sieve of Atkins function some unexpected behaviour was encountered. It took quite a bit of time to find 2 causes:

- ORI instruction does not behave as it suppose to.
- 16bit modulus function runs into infinite loop at specific parameters because of BGE (Branch greater than) being used instead of BGT (Branch greater or equal).

Difficulties with tasks management due to COVID-19 chaos.

## 3 Failure Risk Assessment

There are no updates on failure risk assessment.

## 4 Updated Safety Risk Assessment

There are no updates on safety risk assessment.

## 5 Help and Advice Needed

At this state no help is needed, and any issues and advices are sorted out and discussed in weekly supervisor meetings.

6 Updated Schedule

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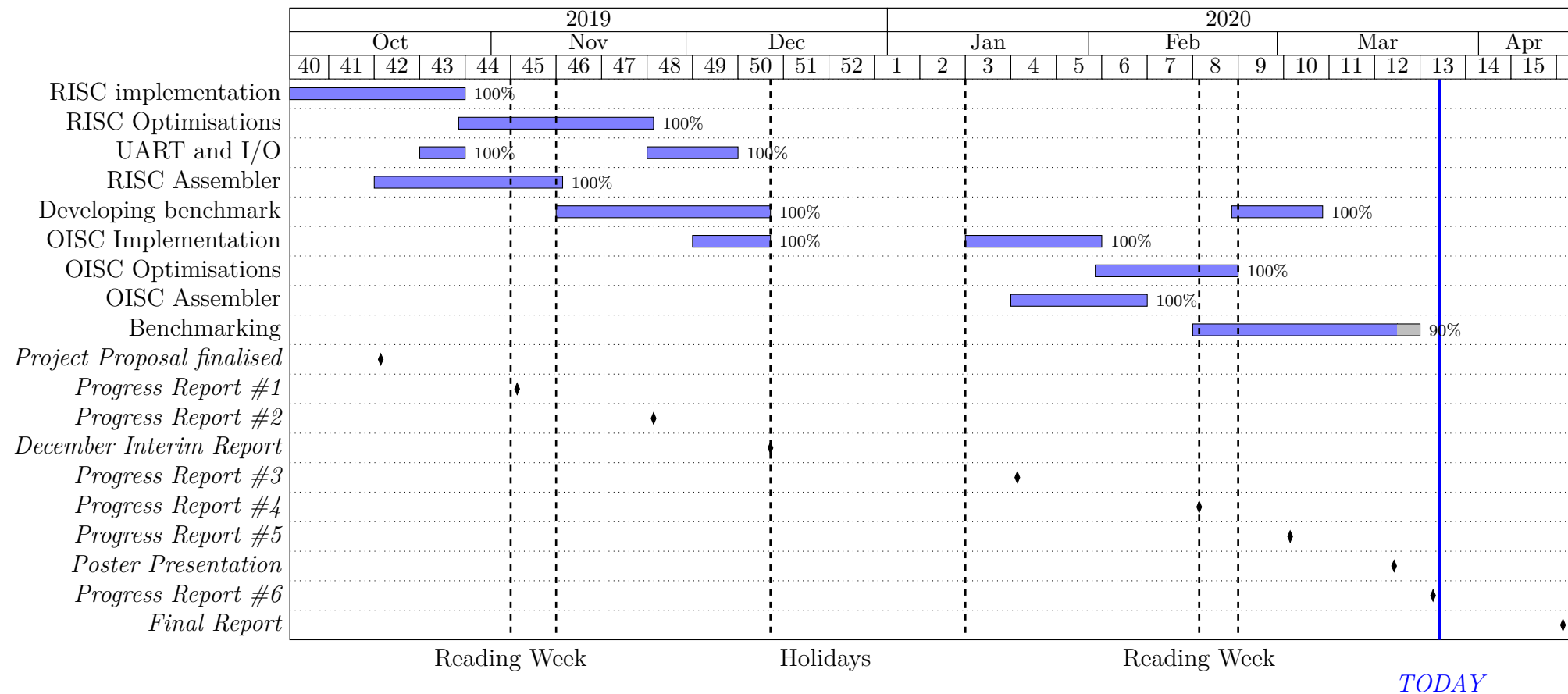


Table 1: Updated project schedule Grantt chart